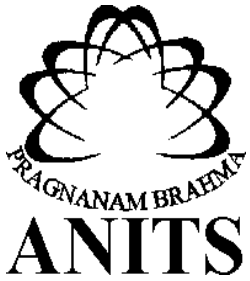
ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY & SCIENCES
(Affiliated to Andhra University Accredited by NBA, UGC Autonomous)
Sangivalasa-531162, Bheemunipatnam Mandal, VisakhapatnamDt.
Phone: 08933-225084, Fax: 08933-226395
www.anits.edu.in principal@anits.edu.in hod_ece@anits.edu.in



Department of Electronics and Communication Engineering

Vision and Mission of ANITS

Vision

ANITS envisions to emerge as a world-class technical institution whose products represent a good blend of technological excellence and the best of human values.

Mission

To train young men and women into competent and confident engineers with excellent communicational skills, to face the challenges of future technology changes, by imparting holistic technical education using the best of infrastructure, outstanding technical and teaching expertise and an exemplary work culture, besides molding them into goodcitizens.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING – ANITS

Department was started with UG program in 2001 with an intake of 60, and subsequently enhanced to 90 in 2003 and to 120 in 2005 and to 180 in 2014. PG program (M.Tech) in Communication Systems with an intake of 18 has been sanctioned from the academic year 2011-2012. The Department was accredited by NBA.

FACULTY:

A team of highly qualified faculty members, comprises of 33 staff members with 3 Professors, 3 Associate Professors and 27 Asst. Professors, One Instrumentation Engineer, 1 senior technician and 3 Technicians. There are 10 Ph.D holders in the department and 21 faculty are pursuing Ph.D

Research Center:

The department is recognized as Research Center by Andhra University and currently there are 12 Ph.D scholars guided by the faculty of the department.

MOU:

The Memorandum Of Undestanding (MOU) is executed between M/S Avantel Limited, incorporated under the laws of Indian Companies Act, 1956, having its registered office at plot no.47/P,APIIC Industrial Park, Gambheeram(V), Anandapuram (M), Visakhapatnam-531163, who is specialist in Defense Electronics, Satellite Communication technologies and Embedded Systems,and Anil Neerukonda Institute Of Technology & Sciences, Affiliated to Andhra University and Accredited by NBA, Sangivalasa-531162, Bheemunipatnam Mandal, Visakhapatnam , effective from Nov 2016 for three years.

The Memorandum Of Undestanding (MOU) is executed between M/s Appleton Innovations, Visakhapatnam and Anil Neerukonda Institute Of Technology & Sciences, Affiliated to Andhra University and Accredited by NBA, Sangivalasa-531162, Bheemunipatnam Mandal, Visakhapatnam , effective from March 2019.

The Memorandum Of Undestanding (MOU) is executed between M/S EffetronicsPvtLimited , Vijayawada and the department of ECE, ANITS, for 3 years, effective from 2017.

Library and Internet Facility:

Department has an exclusive Departmental library with around 700 Volumes and consisting of E-Learning resources like NPTEL. Department is provided with internet facility with 4 Mbps speed.

LABS & ICT Class Rooms:

The Department has well equipped 8 labs like DSP/VHDL Lab, Microprocessors and Applications Lab, Communication Lab, Electronic Devices and Circuits Lab-1, Electronic Devices and Circuits Lab-2, Microwave and Antennas lab, Project lab and Simulation Lab. The department has a Seminar hall with Projector facility and there are 5 lecture rooms with Projector facility.

CLUBS:

To encourage the extra-curricular activities of the students and to make them think out of box, the department of ECE has active student cum faculty clubs like Creativity & Innovations Club, Higher Education Club, Green Club, Wall magazine Club, Yoga Club, Sports Club and Cultural Club.

Vision

To become a center of excellence in Education and Research and produce high quality engineers in the field of Electronics and Communication Engineering to face the challenges of future technology changes.

Mission

To achieve the vision, the department will

Transform students into valuable resources for industry and society by imparting contemporary technical education.

Develop interpersonal skills and leadership qualities among students by creating an ambience of academic integrity to participate in various professional activities.

Create a suitable academic environment to promote research attitude among students.

PROGRAM EDUCATIONAL OBJECTIVES (PEOS)

PEO - 1 Graduates excel in their career in the domains of Electronics, Communication and Information Technology.

PEO -2 Graduates will practice professional ethics and excel in professional career through interpersonal skills and leadership qualities.

PEO – 3 Graduates demonstrate passion for competence in higher education, research and participate in various professional activities

PROGRAM OUTCOMES (POs)

PO1: An ability to independently carry out research /investigation and developmentwork to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program.The mastery should be at a level higher than therequirements in the appropriate bachelor program

PROGRAM SPECIFIC OUTCOMES (PSOS)

PSO 1. Acquire competency in VLSI Design, IC Fabrication, Testing, Verification and prototype development focusing on applications.

PSO 2. Integrate multiple sub-systems to develop Embedded Systems Applications.

ACADEMIC REGULATIONS FOR M.TECH PROGRAM UNDERAUTONOMOUS STATUS

W.E.F. THE ADMITTED BATCH OF 2015-16

I. Admissions:

Admissions into first year of M.Tech Program of the Institute will be as per the norms stipulated by Andhra University & Andhra Pradesh State Council for Higher Education (APSCHE), Govt. of Andhra Pradesh.

II. ProgramsOffered:

The following are the M.Tech. programs offered by the Institute.

01. Control Systems Engineering – EEEDepartment
02. Computer Science and Technology – CSE Department
03. Communication Systems – ECEDepartment
04. Machine Design – Mech. EnggDepartment

III. Structure Of The M. Tech.Program:

The normal duration of the course is 2 academic years for M.Tech Degree. Candidates should pursue a regular course of study, as detailed below, for not less than two academic years which consists of 4 semesters and should fulfil the academic requirements and pass all the prescribed examinations for the award of thedegree.

The curriculum of M.Techprogram is designed to have a total of about 68 credits of which a student should acquire a minimum of 66 credits to get the degree awarded. If a student earns all the total credits, then the best 66 credits are considered to determine the final CGPA. However, the credits which a student can forego will be in accordance with the mandatory courses and electives offered by the individualdepartments.

IV. Duration of theProgram:

The duration of the program is 2 academic years consisting of 2 semesters in each academic year. A student is permitted to complete the Program in a stipulated time frame of 4 consecutive academic years from the date of initial admission and if fails will forfeit his seat in M. TechProgram.

V. Medium ofInstruction:

The medium of instruction and examination is English.

VI. Minimum InstructionDays:

Each semester normally consists of a minimum of 16 weeks of instruction.

VII. AcademicCalendar:

The dates of all important events, such as commencement of class work, examinations, vacations, etc., during the academic year will be specified in the Academic Calendar of the Institute, as approved by the Academic Council.

VIII. Examinations & EvaluationProcess:

The performance of a student in each semester shall be evaluated course-wise with a maximum of 100 marks each for theory and practical courses.

(a) TheoryCourse:

For all lecture based theory courses, the assessment shall be for 40 marks through internal evaluation and 60 marks through external semester-end examination of three hours' duration.

The sessional marks shall be awarded through internal evaluation by the teachers concerned based on the continuous assessment which includes class tests, quiz, viva-voce, assignments, student regularity, two mid-examinations etc., according to a scheme notified by the department at the beginning of thesemester.

Out of the 40 internal evaluation marks, 20 marks are assigned for 2 internal-mid exams, 10 marks are assigned for assignments, 5 marks are assigned for projects/ casestudies

/quiz/tests and 5 marks are assigned for attendance. The average of 2 internal-mid exams isconsidered for the 20 marksallocated.

Under any circumstances, no re-examination shall be conducted for the internal mid examinations.

ii) Externalevaluation:

The question paper shall be set externally and the answer scripts are valued through a double valuation system.

The average of the two valuations will be taken for award of marks. In case, the difference of the marks obtained in the two valuations is more than 20% then a third examiner shall value the script. Out of the three valuations, the average of marks obtained in third valuation and the marks obtained nearer to third valuation out of first two valuations shall be considered. No revaluation for any subject/course shall be entertained as already double valuation system is in existence. However, recounting is allowed on the request of the candidate on payment of specified fee. Challenge valuation shall also be entertained on payment of specifiedfee.

(b) LaboratoryCourse:

Each student will perform about 10 to 12 experiments in each laboratory course. Laboratory course will be evaluated for 100 marks, out of which 50 marks are for external examination and 50 marks are for internal evaluation. The internal marks are awarded based on continuous assessment, record work, internal lab examination and student regularity. The external examination will be conducted by two examiners, one of them being laboratory class teacher as internal examiner (nominated by the Principal on recommendation of HOD) and an external examiner nominated by the Principal from the panel of experts recommended by theHOD.

A candidate shall be declared to have passed in any theory subject/course if he secures not less than 40% in external theory examination and also a minimum of 50% of total marks of that course which assures a minimum of 'E' grade.

A candidate shall be declared to have passed in any practical course if he secures not less than 50% of total marks of that course which assures a minimum of 'E' grade.

Any student appearing for the semester-end practical examination is eligible only if he submits the bonafide record certified by the laboratory class teacher and the HOD.

(C) Thesis Work:

The thesis work shall be carried out in two semesters of one full academic year. The students will be allotted for thesis by the Department committee to various faculty members who act as guides. However, a student can carry-out his thesis work either in the Department or in any other industry / research institute. In any such request to carryout thesis work outside the college, the permission of the Principal and an internal guide is mandatory. Such students should report to the internal guide once in a week essentially through mail or othercommunication.

The progress report of such work is to be submitted by the guide/external guide every month to the HOD. If the work is not found satisfactory, the HOD has the right to call back the student with the permission of the Principal. In any case the time and conditions for submission of the thesis will be same as for the regular candidates working in the college.

The third semester work is evaluated internally by the committee nominated by the HOD consisting a minimum of four members (concerned in area of specialization) including the HOD. If the work is not satisfactory, the candidate has to improve to the satisfaction of the committee within one month from the end of the semester to carry on his fourth semester work. If he fails to satisfy the committee in the second attempt he has to get readmitted into the third semester as per college norms. The grades will be awarded just as in the case of laboratory work. An internal viva voce by a committee nominated by the HOD is a prerequisite for the submission of the thesis. The fourth semester evaluation will be done through the viva voce examination on the thesis by a board consisting of the following four examiners after submission of the thesis by the candidate duly certified by the Guide and theHOD.

1. The Head of the Department asChairman
2. Senior Professor in theDepartment
3. Internal Guide and External Guide (ifany)
4. External examiner nominated by the Principal from a panel recommended by the HOD.

The panel of the external subject experts shall be submitted to the Principal by the HOD in mutual consent with the guide and other subject experts of the Department.

The valuation of the thesis shall be as specified in the scheme of examination of the laboratory course.

If the candidate fails in the viva voce examination of the thesis, he has to reappear for the viva voce. The candidate has to bear the charges for re-conducting the viva voce.

The prerequisite for submission of the M.Tech.thesis is that one should have published a paper in a reputed international journal/ proceedings of an annual conference.

IX. AttendanceRegulations:

Attendance of a student is computed by considering total number of periods conducted in all courses as the denominator and the total number of periods actually attended by the student in all courses, as the numerator. It is desirable for a student to put in 100% attendance in all the subjects. However, a candidate shall be permitted to appear for the semester end examination provided he/she maintains a minimum of 75% overall attendance in thesemester.

The shortage of attendance on medical grounds can be condoned up to a maximum of 9% provided the student puts in at least 66% attendance and provided the Principal issatisfied with the genuineness of the reasons. The Medical Certificates are to be submitted to the Head of the Department when the candidate reports to the classes immediately after the leave. Certificates submitted afterwards shall not beentertained.

Condonation fee as fixed by the college for those who put in attendance between ≥ 66% and <75% shall be charged before the semester-endexaminations.

In the case of students who participate in co-curricular, extra-curricular activities like student seminars, N.S.S, N.C.C, Inter-collegiate tournaments and any such other activities involving the representation of the Institute, with the prior approval of the Principal, the candidate may be deemed to have attended the classes during the actual period of such activity, solely for the purpose ofattendance.

A student, who could not satisfy the minimum attendance requirement of 66% in any semester, shall be declared 'Detained'. He/she is not eligible to appear for the semester end examinations. He will not be promoted to the next semester and shall have to repeat that semester with the next batch(es) of students. Such students who are detained and seek readmission, should submit undertaking/declaration that they will abide by the regulations existing at the time ofreadmission.

X. Minimum AcademicRequirements:

The following academic requirements have to be satisfied in addition to the attendance requirements mentioned in item No. IX.

- A student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted to each theory subject if only he secures not less than 40% marks in the semester-end examination and a minimum of 50% marks in the sum of the internal evaluation and semester-end examination taken together. In the labs/projects, the student should secure a minimum of 50% marks in the external examination and a minimum of 50% marks in the sum of internal evaluation and external examination evaluation takentogether.

- A student will be promoted to the next semester, if only he satisfies the minimum attendancerequirement.
- Students, who fail to complete their two year course study within Four academic years from the year of their admission or fail to acquire the credits stipulated for the course shall forfeit their seat in M. Tech course and their admission shall stand cancelled.

XI. Award OfGrades:

The absolute grading system is adopted as follows:

S.No.	Range of Marks {%}	Grade	Description	Grade Points
1	90-100	O	Outstanding	10
2	80-89	A	Excellent	9
3	70-79	B	Very Good	8
4	60-69	C	Good	7
5	55-59	D	Fair	6
6	50-54	E	Satisfactory	5
7	49 and below	F	Fail	0
8	The grade 'I' represents absent (subsequently changed into pass or higher grades.)	I	Absent	0

The performance of a student at the end of the each semester is indicated in terms of Semester Grade Point Average (SGPA). The SGPA is calculated as below:

$$SGPA = \frac{\Sigma \text{ (Credits of a course x Grade points awarded for a course)}}{\Sigma \text{ (Credits of a course)}}$$

SGPA is calculated for the candidates who have passed in all the courses in that semester.

Cumulative Grade Point Average (CGPA) will be calculated from II semester onwards up to the final semester and its calculation is similar to that of SGPA, considering all the courses offered from the first semesteronwards.

CGPA is calculated for those who clear all the courses in all the previous semesters.

XII. Award ofClass:

For the award of class, a total of best 74 credits are considered. A candidate, who becomes eligible for the award of M.Tech.Degree, shall be placed in one of the following classes.

S.No.	Class	CGPA
1	First Class with Distinction	7.5 or more*
2	First Class	6.5 or more but less than 7.5
3	Second Class/Pass	5.0 or more but less than 6.5

***First class with Distinction will be awarded only to those students who clear all the subjects of the program in first attempt of regularexaminations.**

The CGPA can be converted to aggregate percentage by multiplying CGPA with 10, in case of requirement by any other university or for any otherpurpose.

XIII. Eligibility for Award of M.Tech.Degree:

A student shall be eligible for the award of the M.Tech degree if he/she fulfils all the following conditions:

1) Registered and successfully completed all the components prescribed for eligibility in the program of study to which he/she is admitted within the stipulatedperiod,
2) Obtained CGPA greater than or equal to 5.0 (Minimum requirement forPass),
3) No disciplinary action is pending against him/herand
4) Has no dues to the Institute includinghostels.

XIV. Malpractices:

The Controller of Examinations/Dean of Examinations shall refer the cases of suspected malpractices in mid examinations and semester-end examinations to Malpractice Enquiry Committee constituted by the Institute. Such committee shall follow the approved scales of punishment. The Principal shall take necessary final action against the erring students based on the recommendations of thecommittee.

XV. Amendments toRegulations:

The Institute may, from time to time, revise, amend, or change the Regulations, Schemes of Examinations, and / or Syllabi and the changes or amendments made shall be applicable to all the students with effect from the dates notified by theInstitute.

XVI. General:

(i) Where the words 'he', 'him', 'his', occur in the regulations, they include 'she', 'her','hers'.

(ii) The academic regulation should be read as a whole for the purpose of any interpretation.

(iii) In case of any doubt or ambiguity in the interpretationof the above rules, the decision of the Principal isfinal.

R-23 COURSE STRUCTURE

M TECH (VLSI AND EMBEDDED SYSTEMS)

DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING: ANITS

I Year – I Semester

Course number	Name of the course	Periods per week		Max. marks		Credits
		Lec.	Lab	Sess.	Exams	
23VE111	Reconfigurable System Design	3	—	40	60	3
23VE112	Embedded Systems and IoT applications	3	—	40	60	3
23VE113	Elective-I	3	—	40	60	3
23VE114	Elective-II	3	—	40	60	3
23VE115	Research Methodology and IPR	3	—	40	60	2
23VE116	IOT Applications LAB	—	3	50	50	2
23VE117	Reconfigurable system design lab	—	3	50	50	2
23VE118	Audit Course I	3	—	40	—	0
TOTAL		**18**	**6**	**340**	**400**	**18**

I Year – IISemester

Course number	Name of the course	Periods per week		Max. marks		Credits
		Lec.	Lab	Sess.	Exams	
23VE121	Low Power VLSI Design	3	—	40	60	3
23VE122	MOS Device Modelling	3	—	40	60	3
23VE123	Elective-III	3	—	40	60	3
23VE124	Elective - IV	3	—	40	60	3
23VE125	Mixed signal Embedded System Design Lab	—	3	50	50	2
23VE126	VLSI Lab	—	3	50	50	2
23VE127	Audit Course II	3	—	40	—	0
23VE128	SEMINAR	3		100		2
TOTAL		**18**	**6**	**400**	**340**	**18**

II Year – ISemester

Course number	Name of the course	Periods per week	Max. marks		Credits
			Sess.	Exams	
23VE211	Project phase I	12	100		10
23VE212	SEMINAR	3	100		2
23VE213	MOOC 1				2
23VE214	MOOC 2				2
TOTAL		**17**	**200**		**16**

II Year – II Semester

Course number	Name of the course	Periods per week	Max. marks			Credits
				internal	External	
23VE221	Project phase II	12	Recommended with grade O,A,B,C,D /Not recommended	100	100	16

The prerequisite for submission of the M Tech thesis is that one should communicate his/her work to any referred journal or Publication in a conference/journal.

Elective I:

A. Microsystems-Materials, Processes and Devices
B. Physics of semiconductor devices
C. Compound Semiconductor Devices And Technology
D. Nano-Electronics

Elective II:

A. Analog IC Design
B. Introduction to CAD for VLSI
C. Digital VLSI Design
D. VLSI Digital Signal Processing

Elective III:

A. Embedded Control Systems
B. Real Time Operating Systems
C. Embedded Computing Systems
D. Embedded Automotive Systems Networking

ELECTIVE IV:

A. VLSI for wireless communications
B. Design for Testability
C. Testing and Verification of VLSI Circuits
D. Hardware Security

Audit courses:

1. Advanced Mathematics
2. English for Research PaperWriting
3. Disaster Management
4. ValueAddition
5. Constitution of India
6. PedagogyStudies
7. Stress Management byYoga
8. Personality Development through Life EnlightenmentSkills

RECONFIGURABLE SYSTEM DESIGN	
23VE111	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

DE

COURSE OBJECTIVES

1. To learn designing using HDLs in FPGA platforms

COURSE OUTCOMES

By the end of the course student will be able to:	
1	**Gain comprehensive** knowledge of Reconfigurable Computing Systems
2	**Familiarize** with the Basic concepts of hardware description languages
3	**Acquire** knowledge of different VHDL programming constraints
4	**Apply** the knowledge of Reconfigurable architectures like FPGAs in designing and implementing digital ICs
5	**Perform** High Level Compilation VLSI/FPGA Design for different applications.

Mapping of Course Outcomes with Program Outcomes& Program Specific Outcomes:

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	3	-
	2	3	2	3	3	-
	3	3	2	3	3	-
	4	3	2	3	3	-
	5	3	2	3	3	-

SYLLABUS

UNIT 1 **10 hrs**

Introduction to Reconfigurable Computing Systems: Objectives, Expectations, Logistics, characterization of Reconfigurable Computing & Reconfigurable Hardware, Reconfigurable Software

UNIT 2 **10 hrs**

Basic concepts of hardware description languages (VHDL , Verilog HDL), logic and delay modeling, Structural, Data-flow and Behavioral styles of hardware description, Architecture of event driven simulators, Syntax and Semantics of VHDL, Variable and signal types, arrays and attributes,

UNIT 3 **10 hrs**

Operators, expressions and signal assignments, Entities, architecture specification and configurations, Component instantiation, Concurrent and sequential constructs, Use of Procedures and functions, Synthesis of logic from hardware description.

UNIT 4 **10 hrs**

Types of Reconfiguration, Details study of FPGA, Design tradeoffs, Bidirectional wires and switches, FPGA Placement: Placement Algorithms, FPGA Routing, Timing Analysis, Network Virtualization with FPGAs, On-chip Monitoring Infrastructures, Multi-FPGA System Software, Logic Emulation, Applications,

UNIT 5 **10 hrs**

High Level Compilation VLSI/FPGA Design for Wireless Communication Systems, Reconfigurable Coprocessors, Power Reduction techniques,
A brief idea on SOC, SOPC, PSOC and FPAA.

TEXT BOOKS

1. C. H. Roth, *Digital Systems Design Using VHDL*, Thomson Publications , 2002
2. Scott Hauck and Andre DeHon, *Reconfigurable Computing*, Morgan Kaufmann , 2008

REFERENCE BOOKS

1. R. C. Cofer and B. F. Harding, *Rapid System Prototyping with FPGAs: Accelerating the Design Process*, Elsevier/Newnes , 2005
2. J Bhasker, *A Verilog Primer*, Star Galaxy Publishing

EMBEDDED SYSTEMS AND IOT APPLICATIONS

23VE112	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

Microprocessors & Microcontrollers

COURSE OUTCOMES

By the end of the course, the student will be able to:	
1.	Evaluate the Embedded system design flow from the requirements to the deployment level and analyze the hardware/software tradeoffs involved in the design of embedded systems.
2.	Acquire knowledge of the architecture of Raspberry Pi microcontroller and Install & Configure Raspberry Pi
3.	Explore the IoT conceptual frame work, IoT Architectural view and Understand the Technology behind IOT & Sources of IoT along with M2M communication
4.	Evaluate Design Principles for Connected Devices and analyze Data Enrichment, Data consolidation and device management at gateway
5.	Analyze various protocols of Web communication & Message communication for connected devices and Web connectivity for connected-devices

Mapping of Course Outcomes with Program Outcomes& Program Specific Outcomes:

		PO			**PSO**	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	-	3
	2	3	2	3	-	3
	3	3	2	3	-	3
	4	3	2	3	-	3
	5	3	2	3	-	3

SYLLABUS:

UNIT I: 10 Periods

Introduction to Embedded Systems

Embedded systems overview, Design challenge – optimizing design metrics, Embedded processor technology: General-purpose processors – software, Single-purpose processors – hardware, Application-specific processors; IC technology: Full-custom/VLSI, Semi-custom ASIC (gate array and standard cell), PLD; Design Technology: Compilation/Synthesis, Libraries/IP, Test/Verification, Other productivity improvers;

UNIT II: 12 Periods

Introduction to the Raspberry Pi's Architecture and Setup : History and background of the Raspberry Pi, Basic hardware needed, The microSD card – the main storage and boot device of the Raspberry Pi 2, Installing Screen and Vim, Running tests on the OS and configuration changes

UNIT III: 10 Periods

Internet of Things: An Overview: Internet of things: IoT Definition, IoT Vision, Smart and Hyper connected Devices; IoT conceptual frame work, IoT Architectural view, Technology behind IOT: Server-end Technology, Major Components of IoT System, Development Tools and Open-source Framework for IoT Implementation, APIs and Device Interfacing Components, Platforms and Integration Tools; Sources of IoT: Popular IoT Development Boards, Role of RFID and IoT Applications, Wireless Sensor Networks (WSNs); M2M communication: M2M to IoT, M2M Architecture, Software and Development Tools; Examples of IoT: Wearable Smart Watch, Smart Home, Smart Cities

UNIT IV: 10 Periods

Design Principles for Connected Devices: Introduction, IoT and M2M Systems layers, and design standardization, Communication technologies, Data Enrichment, Data consolidation and device management at gateway, Ease of designing and affordability

UNIT V: 12 Periods

DesignPrinciples for Web Connectivity: Introduction, Web communication protocols for connected devices, Message communication protocols for connected devices, Web connectivity for connected-devices network using

Gateway, SOAP, REST, HTTP RESTful, and Web sockets

Text Books:

1. Frank Vahid, Tony Givargis, *Embedded System Design*, 2nd Edition, John Wiley.
2. Andrew K. Dennis ,*Raspberry Pi Computer Architecture Essentials*,1st edition, Packt publishing,2016
3. Raj Kamal, *INTERNET OF THINGS Architecture and Design Principles*, 1st edition, McGraw Hill Education (India) Private Limited, 2017

Reference Books:

1. David E. Simon, An Embedded Software Primer, Pearson Education
2. Wayne Wolf, Computers as Components-principles of Embedded computer system design, Elsevier

MICROSYSTEMS-MATERIALS, PROCESSES AND DEVICES	
23VE113(A)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites

Physics, Chemistry, Basic electronics

COURSE OBJECTIVES

1. To make the students aware of modern miniatuarized technologies and its utilization to develop various MEMS sensors, actuators, micro devices in different applications

COURSE OUTCOMES

By the end of the course, the student will be able to:	
1.	Acquire the knowledge of Evolution of microelectronics MEMS materials and their properties.
2.	Learn MEMS fabrication process.
3.	Learn the Etching process involved in micro materials.
4.	Acquire the knowledge of bonding, packaging and testing
5.	Learn about the Micro sensors.

Mapping of Course Outcomes with Program Outcomes& Program Specific Outcomes:

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	1	-
	2	3	2	3	1	-
	3	3	2	3	1	-
	4	3	2	3	1	-
	5	3	2	3	1	-

SYLLABUS

UNIT 1 — 12 HRS

Introduction to Microsystems and its applications: Evolution of microelectronics MEMS materials and their properties: Silicon, GaAs, Quartz, Polymers, Smart materials and their mechanical, electrical properties, thin films for micro and nano technologies, Wafer preparation Scaling Laws

UNIT 2 — 12 HRS

Micromachining Technology: MEMS fabrication process: Diffusion, Deposition: Oxidation, Evaporation, Sputtering, CVD Lithography: fundamentals, photoresists, lithography processes, Types: Optical, Electron-beam, focused ion beam, Xray, LIGA process

UNIT 3 — 8 HRS

Etching: bulk and surface micromachining isotropic and anisotropic, wet and dry etching, reactive ion etching and deep reactive ion etching.

UNIT 4 — 8 HRS

Wire bonding, packaging and testing- microassembly, reliability studies.
Transduction mechanism for MEMS devices: Electrostatic, thermal, magnetic etc.

UNIT 5 — 10 HRS

Micro Sensors: Thermal sensors, Radiation sensors, Mechanical sensors, Inertial sensors, Modern applicatinons of MEMS in Energy harvesting and Biomedical applications, BioMEMS and Biosensors.

TEXT BOOKS

1. G. K. Ananthasuresh, K. J. Vinoy, and S. Gopalakrishnan, *Micro and Smart Systems*, Wiley
2. N. Maluf, *An Introduction to Microelectromechanical systems Engineering*, Artech House

REFERENCE BOOKS

1. M. Madou, *Fundamentals of Microfabrication*, CRC Press
2. J.W Gardner, *Micro sensors, MEMS and Smart devices*, John Wiley & sons

JOURNAL AND CONFERENCES

1. Journal of Microelectromechanical Systems
2. Microsystem Technologies

PHYSICS OF SEMICONDUCTOR DEVICES	
23VE113(B)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

Physics, Chemistry, Basic electronics

Course objectives:

1. To learn about Basics of Semiconductor Devices.
2. To learn about material properties of III-V and IV-IV compound semiconductormaterials.
3. To learn about Layers.
4. To learn about high electron mobility transistors and optoelectronic devices.

Course outcomes:

At the end of the course, students will be to
1.Acquire knowledge about Basics of Semiconductor Devices
2. Acquire knowledge about Quantitative Theory of P-N Junctions.
3. Acquire knowledge about Oxide Layers
4. Illustrate the working principles of HEMTs.
5. Illustrate the working principles ofBJTand HBT

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	1	-
	2	3	2	3	1	-
	3	3	2	3	1	-
	4	3	2	3	1	-
	5	3	2	3	1	-

UNIT 1 : BASICS OF SEMICONDUCTOR DEVICES **10 hrs**

Importance of semiconductor devices and their diverse applications.Introduction to semiconductors, concept of energy bands and how bands form.Effective mass of electrons, E-k diagram.Concept of holes.Concept of Fermi level, Fermi-Dirac distribution.Doping (extrinsic & intrinsic semiconductor), density of states. Equilibrium electron-hole concentration, temperature-dependence. Carrier scattering and mobility, velocity saturation, Drift-diffusion transport

UNIT 2 :QUANTITATIVE THEORY OF P-N JUNCTIONS **10 hrs**

Excess carrier decay & recombination, charge injection, continuity equation, quasi-Fermi level p-n junction: static behaviour (depletion width, field profile), p-n junction under forward & reverse bias, current equations, generation-recombination current and reference to typical devices.

UNIT 3: OXIDE LAYERS **10 hrs**

Zener and avalanche breakdown, Capacitance-voltage profiling, metal/semiconductor junction – Ohmic and Schottky contacts, reference to device applications. MOS capacitor, charge/field/energy bands, accumulation, inversion, C-V (high and low frequencies), deep depletion, Real MOS cap: Flat-band & threshold voltage, Si/SiO2 system.

UNIT 4: MOSFET AND HEMT **10 hrs**

MOSFET: structure and operating principle, derivation of I-V, gradual channel approximation, substrate bias effects, sub-threshold current and gate oxide breakdown. Control of threshold voltage, short channel effects. Moore's Law and

CMOS scaling Introduction to compound semiconductors & alloys, commonly used compound semiconductors, heterostructure band diagrams and basics of MODFET & HEMT, introduction to quantum well, applications of heterostructure device technologies

UNIT 5: BJT AND HBT **10 hrs**

BJT: working principle, DC parameters and current components, base transport factor, Early Effect, charge control equation & current gain, need for HBT. Applications of BJTs/HBTs in real-life. (Basics of) - transistors for high-speed logic, transistors for high frequency (RF), transistors for high power switching, transistors for memories, transistors for low noise, transistors for the future

REFERENCES

1. Solid State Electronic Devices, by Ben Streetman and Sanjay Banerjee, Prentice Hall.
2. Introduction to Semiconductor Materials and Devices, by M. S. Tyagi, Wiley Publications.
3. Physics of Semiconductor devices; S.M.Sze, Wiley Publications.
4. Fundamental of Semiconductor Devices;K.N.Bhat&M.K.Achuthan , Tata McGraw-Hill Education India

COMPOUND SEMICONDUCTOR DEVICES AND TECHNOLOGY	
23VE113(C)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

Physics, Chemistry, Basic electronics

Course objectives:

1. To learn about basic device parameters for high frequency, high power, andoptoelectronic applications.
2. To learn about material properties of III-V and IV-IV compound semiconductormaterials.
3. To learn about high frequency device operations.
4. To learn about high electron mobility transistors and optoelectronic devices.

Course outcomes:

At the end of the course, students will be to

1.Acquire knowledge about various device parameters for high power and highfrequency, and optoelectronics applications.

2. Acquire knowledge about III-V and IV-IV compound semiconductor materialproperties.

3. Illustrate the working principles of MESFETs.

4. Illustrate the working principles of HEMTs.

5. Acquire knowledge about compound semiconductors based optoelectronic devices.

Mapping of Course Outcomes with Program Outcomes& Program Specific Outcomes:

		PO			**PSO**	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	1	-
	2	3	2	3	1	-
	3	3	2	3	1	-
	4	3	2	3	1	-
	5	3	2	3	1	-

UNIT I **12 HRS**

Important parameters governing the high-speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration, and temperature; important parameters governing the high-power performance of devices and circuits: Break down voltage, resistances, device geometries, doping concentration, and temperature.

UNIT II **12 HRS**

Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices, outline of the crystal structure, dopants and electrical properties such as carrier mobility, velocity versus electric field characteristics of these materials, electric field characteristics of materials and device processing techniques, Band diagrams, homo and hetero junctions, electrostatic calculations, Band gap engineering, doping, Material and device process technique with these III-V and IV – IV semiconductors.

UNIT III **12 HRS**

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts,

Schottky barrier diode, Metal semiconductor Field Effect Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current. Velocity overshoot effects and the related advantages of GaAs, InP and GaN based devices for high-speed operation. Sub threshold characteristics, short channel effects and the performance of scaled down devices.

UNIT IV **12 HRS**

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET(MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high-speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices; High Frequency resonant –tunneling devices, Resonant-tunneling hot electron transistors.

UNIT V **12 HRS**

Optical Devices: Fundamentals of compound semiconductor based optical devices, Optical density of States, fundamentals, and formation of Heterostructures devices, Fundamentals of LED, essential band structures of LED. Fundamentals of semiconductor LASER with detail theory.

REFERENCES:

1. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications, Wiley & Sons.
2. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons.
3. David K. Ferry, Ed., Gallium Arsenide Technology, Howard W. Sams& Co., 1985
4. Avishay Katz, Indium Phosphide and Related materials: Processing, Technology and Devices, Artech House, 1992.
5. S.M. Sze, High Speed Semiconductor Devices, Wiley (1990) ISBN 0-471-62307-5
6. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5,
7. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 012-691740-X.

8. Semiconductor Optoelectronic Devices, Bhattacharya Pallab, Pearson

NANO ELECTRONICS	
23VE113(D)	**Credits:3**
Instruction:3Periods&1E/week	SessionalMarks:40
EndExam:3Hours	End ExamMarks:60

ANALOG IC DESIGN

Prerequisites: Nil

CourseOutcomes:

Aftercompletionofthe coursethe studentwill beable to

CO1 Explain the fundamental of Nano electronics, CMOS scaling with its limits and basics of semiconductor electronics

CO2 Explain the fundamental of quantum mechanics behind Nano electronics,

CO3 Understand the Nano electronics &Nanocomputer architectures

CO4 Design and analysis of Nano structure and Nano electronics devices using MOSFET, FINFETs, Tunelling FET, Vertical FET, Junctionless Transistor, Single electron transistors

CO5 Describe resonant tunneling transistor, optoelectronic, and spintronic devices.

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	1	-
	2	3	2	3	1	-
	3	3	2	3	1	-
	4	3	2	3	1	-
	5	3	2	3	1	-

SYLLABUS

UNIT I: **10 hrs**

Introduction: Why Nanotechnology and nanoelectronics, Moore's law, Basics of Semiconductor electronics.

UNIT-II: **10 hrs**

Basics of Quantum Mechanics: Wave nature of particles and wave-particle duality, Pauli-exclusion principle, wave functions and Schrodinger's equations. Quantum dots, wires, and wells.Principles of optical devices.

UNIT-III: **10 hrs**

Nano electronics &Nanocomputer architectures: Introduction to Nanocomputers, Nanocomputer Architecture, Quantum DOT cellular Automata (QCA), QCA circuits, Single electron circuits, molecular circuits, Logic switches – Interface engineering – Properties (Self-organization, Size-dependent) – Limitations.

UNIT-IV: **10 hrs**

Nano semiconductor devices: Overview of MOS and MOSFET, Scaling and Nano MOSFET, Interconnects, FINFET, Tunelling FET, Vertical FET, Junctionless Transistor, Single electron transistors

UNIT-V: **10 hrs**

Spintronics: Introduction, Overview, History & Background, Generation of Spin Polarization Theories of spin Injection, spin relaxation and spin dephasing, Spintronic devices and applications, spin filters, spin diodes, spin transistors.

TEXT BOOKS

1.Nanoelectronics&Nanosystems: From Transistor to Molecular & Quantum Devices: Karl Goser, JanDienstuhl and others.

2. Nano Electronics and Information Technology: Rainer Waser

3.D.A. Neamen, Semiconductor Physics & Devices, TMH, 2003.

REFERENCES

1. Concepts in Spintronics – SadamichiMaekawa

2. Spin Electronics – David Awschalom

23VE114(A)	Credits:3
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:
Analog circuits, digital circuits
COURSE OUTCOMES

1. To Model the MOS transistors considering different electrical effects.
2. To Design and Analyze the basic MOS amplifiers.
3. To Design and analyze current mirror cicruits.
4. To Analyze and design analog circuits such as Differential Amplifier, OP-AMP..
5. To explore nanometer design strategies and band gap references.

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	3	-
	2	3	2	3	3	-
	3	3	2	3	3	-
	4	3	2	3	3	-
	5	3	2	3	3	-

SYLLABUS

UNIT 1 **8 hrs**

General consideration of MOS devices – MOS I/V Characteristics – Second order effects – MOS device models. Short-Channel Effects and Device Models - Scaling Theory , Short-Channel Effects, MOS Device Models (short channel), Process Corners

UNIT 2 **10 hrs**

Basic Concepts – Common source stage- Source follower- Common gate stage- Cascode stage. Single ended and differential operation- Basic Differential pair- Common mode response- Differential pair with MOS loads- Gilbert Cell.

UNIT 3 **10hrs**

Basic current mirrors- Cascode current mirrors- Active current mirrors- Large and Small signal analysis- Common mode properties.

UNIT 4 **12hrs**

Operational amplifiers: General Considerations- One and Two Stage Op Amps- Gain Boosting- Comparison- Common mode feedback- Input range limitations- Slew rate- Power Supply Rejection- Noise in Op Amps- General consideration of stability and frequency compensation- Multipole system- Phase margin- Frequency compensation- Compensation of two stage op Amps- Other compensation techniques.

UNIT 5 **10 hrs**

Bandgap References:General Considerations, Supply-Independent Biasing, Temperature-Independent References, PTAT Current Generation, Constant-Gm Biasing, Speed and Noise Issues, Low-Voltage Bandgap References

TEXT BOOKS

1. B. Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill , 2002
2. P.E. Allen and D.R.Holberg, *CMOS Analog Circuit Design*, Oxford University Press , 2004

REFERENCE BOOKS

3. R.Gregorian and G.C.Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley and Sons , 2004
4. R.J.Baker, H. W. Li, D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, PHI , 2002

INTRODUCTION TO CAD FOR VLSI	
23VE114(B)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:
Digital Electronics, VLSI design

Course objectives:
- Make the student to familiar with VLSI design automation
- Students should develop algorithms for VLSI CAD.

Course Outcomes:

By the end of the course student will be able to:	
1	**Gain comprehensive** knowledge of VLSI design flow and automation
2	**Familiarize** with the high level synthesis process
3	**Acquire** knowledge of logic synthesis process.
4	**Explain** algorithms for floorplanning, partitioning and placement
5	**Explain** algorithms for routing.

		PO		**PSO**		
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	2	-
	2	3	2	3	2	-
	3	3	2	3	2	-
	4	3	2	3	2	-
	5	3	2	3	2	-

SYLLABUS

UNIT I: **9 Periods**

INTRODUCTION TO DESIGN METHODOLOGIES

The VLSI Design Problem, The Design Domains,Design Actions, Design Methods and Technologies
Quick Tour of VLSI Design Automation Tools:Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools

UNIT II: **9 Periods**

HIGH-LEVEL SYNTHESIS

Hardware Models for High-level Synthesis: Hardware for Computations, Data Storage, and Interconnection, Data, Control, and Clocks
Internal representation of the Input Algorithm: Simple Data Flow, Conditional Data Flow, Iterative Data Flow, Data-flow Graph Representation Allocation, Assignment and Scheduling: Goals and Terminology, A detailed Example, Optimization Issues Some Aspects of the Assignment Problem : Optimization Issues , Graph Theoretical problem Formulation , Assignment by Interval and Circular-arc Graph Coloring , Assignment by Clique Partitioning High-level Transformations

UNIT III: **10 Periods**

LOGIC SYNTHESIS AND VERIFICATION

Introduction to Combinational Logic Synthesis: Basic Issues and Terminology, A Practical Example
Binary-decision Diagrams: ROBDD Principles, ROBDD Implementation and Construction, ROBDD Manipulation, Variable Ordering , Applications to Verification , Applications to Combinatorial Optimization
Two-level Logic Synthesis : Problem Definition and Analysis, A Heuristic Based on ROBDDs

UNIT IV: **9 Periods**

FLOORPLANNING PLACEMENT AND PARTITIONING

FloorplanningConcepts : Terminology and Floorplan Representation , Optimization Problems in Floorplanning Shape Functions and Floorplan Sizing

Placement and partitioning:

Circuit Representation, Wire Length Estimation Types of Placement Problem
Placement Algorithms :Constructive Placement , Iterative Improvement
Partitioning : The Kernighan-Lin Partitioning Algorithm

UNIT V: 8 Periods

ROUTING

Types of Local Routing Problems, Area Routing Channel Routing: Channel Routing Models , The Vertical Constraint Graph , Horizontal Contraints and the Left-edge Algorithm, Channel Routing Algorithms
Introduction to Global Routing: Standard-cell layout, Building-block Layout and Channel Ordering
Algorithms for Global Routing : Problem Definition and Discussion, Efficient Rectilinear Steiner-tree Construction, Local Transformations for Global Routing.

Text Books:

1. Sabih H. Gerez, Algorithms for VLSI Design Automation, JOHN WILEY & SONS,1998

Reference Books:

1. N.A. Sherwani, "Algorithms for VLSI physical design automation", Kluwer Academic Publishers, 1999.

Digital VLSI Design	
23VE114(C)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

Digital electronics and Logic design

COURSE OBJECTIVES

1. To provide in-depth understanding of the VLSI design process and digital integrated circuits.
2. To provide a basic idea on IC manufacturing process and design for manufacturability and testability.
3. To provide in-depth understanding of the VLSI design process and digital integrated circuits.
4. To provide a basic idea on IC manufacturing process and design for manufacturability.

COURSE OUTCOMES

By the end of the course, the student will be able to:	
1.	Acquire the knowledge of different processing stages of VLSI design.
2.	Design different combinational circuits using CMOS gates as well as alternative logic like transmission gates and pass transistors.
3.	Design Different sequential logic circuits and address timing issues.
4.	Design Dynamic logic circuits and Memories and Analyze them.
5.	Acquire the knowledge of design for manufacturability techniques.

Mapping of Course Outcomes with Program Outcomes& Program Specific Outcomes:

		PO			**PSO**	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	3	-
	2	3	2	3	3	-
	3	3	2	3	3	-
	4	3	2	3	3	-
	5	3	2	3	3	-

SYLLABUS

UNIT 1 **10 Hrs**

Introduction to VLSI Design, Overview of VLSI Design Methodologies, VLSI Design Flow, Design Hierarchy, Concepts of Regularity, Modularity and Locality, VLSI Design Styles, Quality Metrics, Packaging, Levels of abstraction and the complexity of design, Challenges of VLSI design: power, timing, area, noise, testability, reliability and yield

UNIT2 **10Hrs**

MOS combinational logic circuits, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates, Complementary Pass Transistor Logic, Transistor sizing in static CMOS, logical effort, Pass-transistor logic, sizing issues.

UNIT 3 **10 Hrs**

Sequential Logic Circuits: Introduction, Static Latches and Registers, Dynamic Latches and registers, Pipelining. Timing issues in Digital Circuits: Timing classification of digital systems, Synchronous Design Timing basics, clock skew, clock jitter and their combine impact.

UNIT 4 **10Hrs**

Dynamic Logic Circuits: Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Logic, Dynamic CMOS Logic, High Performance Dynamic CMOS Circuits, Domino CMOS logic,NP-DominoLogic, MOS memories: Introduction, DRAM, SRAM, Nonvolatile Memory, Flash Memory,

Designing Arithmetic Building Blocks

UNIT5 **10Hrs**

Design for Manufacturability: Process variations, Parametric Yield Estimation and maximization, Worst-case analysis, Performance Variability Minimization. Design for testability: Fault types and models, Controllability and Observability, Ad Hoc Testable Design Techniques Packaging technology

TEXT BOOKS

1. Sung-Mo Kang, Yusuf Leblebici, *CMOS Digital Integrated Circuits*, TMH , 2014
2. Sung-Mo Kang, Yusuf Leblebici, *Digital Integrated Circuits: A Design Perspective*, Pearson , 2012

REFERENCE BOOKS

1. Kamran Eshraghian and Neil Weste, *Principles of CMOS VLSI Design: A Systems Perspective*, Pearson/Addition Wesley
2. J. P. Uyemura, *Introduction to VLSI Circuits and Systems*, Wiley

VLSI DIGITAL SIGNAL PROCESSING	
23VE114(D)	**Credits:3**
Instruction: 3 periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

VLSI Design, Digital IC Design and Digital Signal Processing

COURSE OBJECTIVES

Students undergoing this course are expected to:

- Interpret the pipelining and parallel processing techniques to the VLSI systems
- Analyze the retiming, unfolding & folding concepts for register minimization
- Infer the systolic architectures
- Design and analyze FIR filters circuits for signal processing
- Apply the fast convolution algorithms to signal processing applications

COURSE OUTCOMES

After undergoing the course, students will be able to	
1.	Represent the DSP algorithms and transforms as systems with block, signal flow and data flow diagrams.
2.	Design pipeline and parallel processed FIR filters.
3.	Perform retiming and minimize the registers and solve the systems of inequalities.
4.	Design systolic architecture using canonical mapping and generalized mapping
5.	Design and analyse parallel and pipeline IIR

Mapping of Course Outcomes with Program Outcomes:

		PO			**PSO**	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	3	-
	2	3	2	3	3	-
	3	3	2	3	3	-
	4	3	2	3	3	-
	5	3	2	3	3	-

Justification:

CO1: The students are expected to represent the description of a system (algorithm/equations) in terms of processing blocks with their connections. Students also draw the signal and data flow graphs for the systems described by blocks. This shows clear understanding of the circuits and application of their knowledge of science. It helps in doing projects in VLSI Signal processing that boost their **technical skills** and **employment opportunities** in the domain.

CO2: The students are expected to **Apply** pipelining and parallel processing techniques to **Design** FIR filters. Students are expected to solve the complex problems. It helps in doing projects in VLSI Signal processing that boost their **technical skills** and **employment opportunities** in the domain.

CO3: The students are expected to **analyze** the digital systems for timing and **Apply**the retiming techniques to reduce critical delay and minimize the registers in a system. It helps in doing projects in VLSI Signal processing that boost their **technical skills** and **employment opportunities** in the domain.

CO4: The students are expected **Design** systolic architecture using canonical mapping and generalized mapping. They are expected to convert the given systems into systolic architectures. It helps in doing projects in VLSI Signal processing that boost their **technical skills** and **employment opportunities** in the domain.

CO5: The students are expected to **Apply** pipelining and parallel processing techniques to **Design** IIR filters. It helps in doing projects in VLSI Signal processing that boost their **technical skills** and **employment opportunities** in the domain.

UNIT I	10 Periods
Introduction to Digital Signal Processing Systems: Typical Signal Processing Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.	
UNIT II	**10 Periods**
Pipelining and parallel processing: Iteration bound, Introduction, Pipelining of FIR filters, Parallel Processing, Pipelining and Parallel processing for low power.	
UNIT III	**10 Periods**
Retiming: Definitions and Properties, Solving systems of inequalities, Retiming techniques. **Unfolding and Folding:** Unfolding Algorithm, Properties of unfolding, Critical Path, Unfolding and Retiming, Folding Transformation, Register Minimization techniques.	
UNIT IV	**10 Periods**
Systolic Architecture Design Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Operations and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.	

SYLLABUS

UNIT V	10 periods
Pipelined and Parallel IIR filters: Pipeline Interleaving in Digital Filter, Pipelining in 1^{st} Order IIR Digital Filters, Pipelining in Higher order IIR Digital Filters, Parallel Processing for IIR filters, Combined Pipelining and Parallel processing for IIR digital filters, Low-power IIR Filter Design Using Pipelining and Parallel Processing.	

Text Books:

1. K. K. Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", John Wiley, 1999.

Reference Books:

1. S.Y.Kung, "VLSI Array Processors", Prentice-Hall, 1988

IoT Applications Laboratory	
23VE116	**Credits:2**
Instruction: 3 Practical & 3 O/Week	Sessional Marks:50
End Exam: 3 Hours	End Exam Marks:50

Prerequisites:

Before starting this course, students should have a basic idea of embedded systems and Internet of Things applications.

COURSE OBJECTIVES:

Students will understand the concepts of Internet of Things and can able to build IoT applications.

Course Outcomes:

By the end of the course student will be able to:	
1	Interface various input and output devices with Raspberry pi.
2	Design the minimum system for sensor-based application.
3	Solve the problems related to the primitive needs using IoT.
4	Develop full-fledged IoT application for distributed environment.

Mapping of Course Outcomes with Program Outcomes &Program Specific Outcomes:

		PO			**PSO**	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3		3
	2	3	2	3		3
	3	3	2	3		3
	4	3	2	3		3

SYLLABUS
(List of Experiments)

S.No	Name of the Experiment
1.	Familiarization of Raspberry pi 4 and its installation.
2.	Interface and control LED/Buzzer with Raspberry pi 4.
3.	Interface push button/digital sensors with Raspberry pi 4.
4.	Read the humidity using Raspberry pi 4.
5.	Operate the motor through relay using Raspberry pi 4.
6.	Send the sensor data through Bluetooth using Raspberry pi 4.
7.	Control LED/Buzzer with Raspberry pi 4 using Bluetooth.
8.	Upload and retrieve humidity and temperature data to thingspeak cloud using Raspberry pi 4.
9.	Control the lights in a room using Raspberry pi 4 (based on user requirements).
10.	Control 230 V devices for a threshold temperature using Raspberry pi 4.
11.	Control 230 V devices using Raspberry pi 4 from a remote location.
12.	IoT based Project

Note: Students have to perform minimum of eight experiments (from Exp.1 to 11) and IoT based project.

Text Books:

1. Vijay Madisetti, ArshdeepBahga," Internet of Things A Hands-On- Approach",2014, ISBN:978 0996025515.

REFERENCE BOOKS:

1. Adrian McEwen, “Designing the Internet of Things”, Wiley Publishers, 2013, ISBN: 978-1-118-43062-0
2. Daniel Kellmereit, “The Silent Intelligence: The Internet of Things”. 2013, ISBN 0989973700.

RECONFIGURABLE SYSTEM DESIGN LAB	
23VE117	**Credits:2**
Instruction: 3 Lab periods	Sessional Marks:50
End Exam: 3 Hours	End Exam Marks:50

Prerequisites:

Digital Electronics, VHDL, Verilog.

COURSE OBJECTIVES

- Familiarize with different VLSI design tools.
- Develop the ICs for digital applications with open source VLSI design tools.
- Prepare the prototypes.
- Testing the digital systems.
- Analyze the digital circuits.

COURSE OUTCOMES

After undergoing the course, students will be able to	
	Work with XILINX VLSI design tools.
	Develop the systems for various signal processing and computing applications
	Test and verify the prototypes at system level using XILINX Vivado simulators.
	Analyze and Develop the prototypes of Digital systems on Artix 7 FPGA.

Mapping of Course Outcomes with Program Outcomes:

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	3	-
	2	3	2	3	3	-
	3	3	2	3	3	-
	4	3	2	3	3	-

Syllabus

Cycle 1: Digital Design using HDL.

Experiment 1: Static Display
Experiment 2: Frequency Divider
Experiment 3: Traffic Light Controller
Experiment 4: Design of Memories

Cycle 2: FPGA prototyping using Artix 7

Experiment 1: Familiarization with Artix 7 FPGA
Experiment 2: Implementation of Adders on Artix 7 FPGA
Experiment 3: Implementation of Multipliers on Artix 7 FPGA
Experiment 4: Implementation of Moore and Mealy FSM on Artix 7 FPGA
Experiment 5: Implementation of ALU on Artix 7 FPGA
Experiment 6: Implementation of 8 bit MAC on Artix 7 FPGA

Text Books:

1. JayaramBhasker, "A Verilog Primer", AT&T, Prentice Hall.
2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design And Synthesis", SunSoft Press 1996

Reference Books:

1. ZainalabedinNavabi, "Verilog Digital System Design", 2nd Edition, McGraw-Hill, 2006.

LOW POWER VLSI DESIGN	
ECVES121	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

Digital Electronics, VLSI design

Course objectives:

To make students familiar with power dissipation, power optimization techniques and power estimation in VLSI circuits.

To make student design the power efficient VLSI systems by applying low power design techniques.

Course Outcomes:

By the end of the course student will be able to:

CO Nos.	Course Outcomes
CO1	Explain the sources of power dissipation in CMOS
CO2	Classifythespecialtechniquestomitigatethepower consumptioninVLSIcircuits
CO3	Summarize the power optimization and trade-off techniques in digital circuits.
CO4	Illustrate the power estimation at logic and circuit level
CO5	Explainthesoftwaredesignforlowpowerinvariouslevel

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	2	-
	2	3	2	3	2	-
	3	3	2	3	2	-
	4	3	2	3	2	-
	5	3	2	3	2	-

SYLLABUS

UNITI POWER DISSIPATIONINCMOS 10 hrs

Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFET, gate induced drain leakage– Power dissipation in CMOS: short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design, hierarchy of limits, fundamental limit, material limit, device limit, system limit.

UNIT II POWER OPTIMIZATION USING SPECIAL TECHNIQUES 10 hrs

Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques - CMOS Floating Node: Tristate Keeper Circuit, Blocking Gate, Low Power Bus: Low Swing Bus, Charge Recycling Bus, Delay Balancing - Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning, Pulsed Word line and Reduced bit line Swing

UNIT III DESIGN OF LOW POWER CIRCUITS 10 hrs

Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization : Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops : Self-gating Flip-flop, Combinational Flip-flop, Double Edge Triggered Flip-flop - Low Power Digital Cell Library : Cell Sizes and Spacing, Varieties of Boolean Functions, Adjustable Device Threshold Voltage

UNIT IV POWER ESTIMATION 10 hrs

Modelling of signals - signal probability calculation - Statistical techniques - estimation of glitching power- Sensitivity Analysis-Power estimation using input vector compaction, power dissipation in Domino logic, circuit reliability, power estimation at the circuit level, Estimation of maximum power: test generation based approach,

steepest descent, generic based algorithm based approach

UNIT V SOFTWARE DESIGN FOR LOW POWER 10 hrs

Sources of software power dissipation - software power estimation: Gate level, architecture level, bus switching activity, instruction level power analysis - software power optimization: minimizing memory access costs, instruction selection and ordering, power management - Automated low power code generation – Co-design for low power.

TextBooks

1. KaushikRoyandS.C.Prasad,"LowpowerCMOSVLSIcircuitdesign",Wiley,2000
2. A.P.ChandrasekaranandR.W.Broadersen,"LowpowerdigitalCMOSdesign",Kluwer,1995
3. GaryYeap,"PracticallowpowerdigitalVLSIdesign",Kluwer,1998

Reference Books

1. DimitriosSoudris,ChristiansPignet,CostasGoutis,"DesigningCMOSCircuitsforLow Power", Kluwer,2002
2. J.B.KuloandJ.HLou,"LowvoltageCMOSVLSICircuits",Wiley1999.

MOS DEVICE MODELLING	
23VE122	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites

Physics, Chemistry, Basic electronics

COURSE OBJECTIVES

1. To make the students aware of modern MOS devices and the modelling of their electrical properties for simulation etc.

COURSE OUTCOMES

By the end of the course, the student will be able to:	
1.	Acquire the knowledge of electron and hole densities in equilibrium
2.	Learn about the PN junction in detail
3.	Analyze the MOSFET devices for different transient and equilibrium conditions.
4.	Acquire the knowledge of second order effects in MOSFET
5.	Learn about the MOSFET scaling, Non-uniform doping in channel, SOI MOSFET, Buried channel MOSFET, Fin FET.

Mapping of Course Outcomes with Program Outcomes& Program Specific Outcomes:

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	1	-
	2	3	2	3	1	-
	3	3	2	3	1	-
	4	3	2	3	1	-
	5	3	2	3	1	-

SYLLABUS

UNIT I - ELECTRON AND HOLE DENSITIES IN EQUILIBRIUM (12 hours)

Fermi – Dirac Statistics, Carrier concentration, Fermi level at equilibrium, recombination, Mobility of carriers, charge transport in semiconductors.

UNIT II - PN JUNCTION (12 hours)

PN Junction under thermal equilibrium under applied bias, Transient Analysis, Injection and Transport model, Diode small signal and large signal model.

UNIT III – MOSFET (12 hours)

Operation of Ideal MOS diode, Effects of mobile Ionic charges, Oxide charges and Interface states, C-V Characteristics, Threshold voltage of MOSFET, Bulk charge model, square law method (Level 1 is SPICE), Level 3 model in SPICE, BSIM Models**.**

UNIT IV - SECOND ORDER EFFECTS IN MOSFET (12 hours)

Effect of Gate voltage on carrier mobility, Effect of Drain voltage on carrier mobility, Channel length modulation, Breakdown and punch through, Subthreshold current, Short channel effects., Meyer's model, Small signal model**.**

UNIT V - ADVANCED TOPICS (12 hours)

MOSFET scaling, Non-uniform doping in channel, SOI MOSFET, Buried channel MOSFET, Fin FET.

TEXT BOOKS

1. Nandita Das Gupta, Amitava Das Gupta, "Semiconductor devices, modeling and Technology", Prentice Hall of Indis, 2004.
2. Philip.E.Allen Douglas, R. Hoberg, "CMOS Analog circuit Design", second edition, Oxford Press, 2002.

REFERENCE BOOKS

1. S.M. Sze, “Semiconductor Devices-Physics and Technology”, John Wiley and Sons, 1985.
2. Kiat Seng Yeo, Samir R.Rofail, Wang-Ling Gob, “CMOS/BiCMOS VLSI-Low Voltage, Low Power”, Pearson Education, Low price edition, 2003.

EMBEDDED CONTROL SYSTEMS	
23VE123(A)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Course Objectives: This course is intended to explain the various concepts used in embedded control systems. Students will also familiarize with real time operating systems.

COURSE OUTCOME (CO): The student will be able to

COURSE OUTCOMES:
At the end of the course, students will be able to

1.	Explain the concept of embedded Systems and its architecture
2.	Familiarize with HCS 12 architecture and peripherals.
3.	Elucidate the concept of programming for different interfacing devices of HCS 12
4.	Learn about the Basic Input /Output Interfacing of embedded control systems.
5.	Excel the concepts of Development tools and Programming for embedded control systems.

		PO			**PSO**	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3		3
	2	3	2	3		3
	3	3	2	3		3
	4	3	2	3		3
	5	3	2	3		3

UNIT 1 **10 hrs**

Introduction: Introduction to Embedded Systems, Its Architecture and system Model, Introduction to the HCS12/S12X series Microcontrollers, Embedded Hardware Building Block.

UNIT 2 **10 hrs**

HCS12 System Description and Programming: The HCS12 Hardware System, Modes of Operation, The B32 Memory System, The HCS12 DP256 Memory System,

UNIT 3 **10 hrs**

Exception Processing–Resets and Interrupts, Clock Functions, TIM, RTI, Serial Communications, SPI-Serial Peripheral Interface, I2C, HCS12 Analog-to-Digital Conversion System.

UNIT4 **10 hrs**

Basic Input /Output Interfacing Concepts: Input Devices, Output Devices and their Programming, Switch Debouncing, Interfacing to Motor, LCDs, Transducer, The RS-232 Interface and their Examples.

UNIT5 **10hrs**

Development tools and Programming: Hardware and Software development tools, C language programming, Codewarior tools- Project IDE, Compiler, Assembler and Debugger, JTAG and Hardware Debuggers, Interfacing Real Time Clock and Temperature Sensors with I2C and SPI bus.

Text Books:

1. Barrett, S.F. and Pack, J.D., Embedded Systems, Pearson Education (2008).
2. Haung, H.W., The HCS12 / 9S12: An Introduction to Software and Hardware Interfacing, Delmar

Learning (2007).

Reference Books:

1. Fredrick, M.C., Assembly and C programming for HCS12 Microcontrollers, Oxford University Press (2005).
2. Ray, A.K., Advance Microprocessors and Peripherals – Architecture, Programming and Interfacing, Tata McGraw□ Hill (2007).

REAL TIME OPERATING SYSTEMS	
23VE123(B)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Pre requisites:
CAO, MP & MC, OS

Course Educational Objectives:
The objective of the course is to introduce the principles shared by many real-time operating systems, and their use in the development of embedded multitasking application software.

COURSE OUTCOMES:
At the end of the course, students will be able to

1.	Familiarize with the Operating System concepts.
2.	Learn the basics of real time operating concepts.
3.	Illustrate the Process management such as threads, scheduling etc.
4.	Learn about the inter-process communications and memory management.
5.	Address kernel issues with case studies.

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3		2
	2	3	2	3		2
	3	3	2	3		2
	4	3	2	3		2
	5	3	2	3		2

SYLLABUS

UNIT-I **(10 hrs)**

INTRODUCTION:

Introduction to Operating System: Computer Hardware Organization, BIOS and Boot Process, Multi-threading concepts, Processes, Threads, Scheduling

UNIT-II **(10 hrs)**

BASICS OF REAL-TIME CONCEPTS:

Terminology: RTOS concepts and definitions, real-time design issues, examples, Hardware Considerations: logic states, CPU, memory, I/O, Architectures, RTOS building blocks, Real-Time Kernel

UNIT-III **(10 hrs)**

PROCESS MANAGEMENT:

Concepts, scheduling, IPC, RPC, CPU Scheduling, scheduling criteria, scheduling algorithms Threads: Multi-threading models, threading issues, thread libraries, synchronization Mutex: creating, deleting, prioritizing mutex, mutex internals

UNIT-IV **(10 hrs)**

INTER-PROCESS COMM
UNICATION:

Messages, Buffers, mailboxes, queues, semaphores, deadlock, priority inversion,

PIPES MEMORY MANAGEMENT: - Process stack management, run-time buffer size, swapping, overlays, block/page management, replacement algorithms, real-time garbage collection

UNIT-V **(10 hrs)**

CASE STUDIES:

Case study Linux POSIX system, RTLinux / RTAI, Windows system,

Vxworks, uItron Kernel Design Issues: structure, process states, data structures, inter-task communication mechanism, Linux Scheduling.

TEXT BOOKS:

1. J. J Labrosse, *"MicroC/OS-II: The Real –Time Kernel"*,
Newnes, 2002.

2. Jane W. S. Liu, *"Real-time systems"*, Prentice Hall, 2000.

REFERENCES:

1. W. Richard Stevens, *"Advanced Programming in the UNIX® Environment"*, 2nd Edition, Pearson Education India, 2011.

2. Philips A. Laplante, *"Real-Time System Design and Analysis"*, 3rd Edition, John Wley& Sons, 2004

3. Doug Abbott, *"Linux for Embedded and Real-Time Applications",* Newnes, 2nd Edition, 2011.

EMBEDDED COMPUTING SYSTEMS	
23VE123(C)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:

Microprocessors & Microcontrollers

COURSE OBJECTIVES

1. To design single purpose and general purpose processor design
2. To study the peripherals, bus protocol and memory subsystems
3. To develop skills and get knowledge about designing embedded system.

COURSE OUTCOMES

By the end of the course, the student will be able to:	
1.	CO1: Learn the knowledge of designing computing architectures used in embedded system.
2.	Learn about the CPU peripherals and the bus protocols such as ISA, CAN, LIN, I2C, AMBA etc.
3.	Design the programs and analyze them using different compiler and operating system concepts.
4.	Use the Hardware Accelerators for different real-time applications.
5.	Learn about H/W and S/W co-design embedded multiprocessor DSP Algorithm Design

Mapping of Course Outcomes with Program Outcomes& Program Specific Outcomes:

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3		3
	2	3	2	3		3
	3	3	2	3		3
	4	3	2	3		3
	5	3	2	3		3

SYLLABUS

UNIT 1 **10 Hrs**

Introduction to software design: Requirements, specifications, structural and behavioral descriptions, UML Embedded Processors: Risc, super scalar, and VLIW architectures, ARM and SHARC, Processor and memory organization and Instruction level parallelism, Processor Design

UNIT 2 **10 Hrs**

CPU architectures: Input/Output, interrupts, modes, cache memories Embedded bus architectures: Bus architectures and transactions, Serial interconnects, Networked embedded systems: Bus protocols, I2C bus, CAN bus, AMBA bus, Ethernet, SerDes Internet-Enabled Systems, Design Example-Elevator Controller.

UNIT 3 **10 Hrs**

Program design and analysis: Compilers and optimization. Testing.Performance Analysis. Operating Systems Tasks, context switches, Operating system support (inter-process communication, networking), Scheduling, Development environment.

UNIT 4 **10 Hrs**

Hardware Accelerators: FPGA architectures, RISC IP Cores, Verilog HDL Embedded System Application, design challenge – optimizing design metrics, processor technology, design technology real time-operating system: system modeling, static scheduling, Priority drive scheduling, Synchronization & mutual exclusion (real-time and non-real-time)

UNIT 5 **10 Hrs**

H/W and S/W co-design embedded multiprocessor DSP Algorithm Design: A/D conversion and finite precision analysis, Algorithms for embedded systems: source and channel processing, Portable embedded code. Low Power architectures for embedded systems

TEXT BOOKS

1. W. Wolf, *Computers as Components : Principles of Embedded Computer System Design*, Second Edition, Elsevier/MK, 2005
2. F. Vahid and T. Givargis, *Embedded System Design: A Unified Hardware/Software Introduction*, Wiley, 2002.

REFERENCE BOOKS

1. P. Marwedel, , *Embedded System Design*, Springer, 2006.
2. Steve Heath, *Embedded Systems Design 2nd Edition*, 2002

EMBEDDED AUTOMOTIVE SYSTEMS NETWORKING	
23VE123(D)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites
Microcontrollers and Embedded Systems
OBJECTIVES:
1. To have knowledge in basic of data communication
2. To have a knowledge in Layers of CAN Network

COURSE OUTCOMES:
At the end of the course, students will be able to

1.	Learn about the basics of data communication.
2.	Illustrate the CAN Data Link Layer
3.	Illustrate the CAN Physical Layer
4.	Analyze the CAN protocol controllers
5.	Learn about the CAN higher layer protocols

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3		2
	2	3	2	3		2
	3	3	2	3		2
	4	3	2	3		2
	5	3	2	3		2

UNIT - I **10 hrs**
DATA COMMUNICATION BASICS
Data communication basics - Network communication protocol – Medium access control – Error checking& control – Requirements & applications of field bus systems- Characteristics of CAN
UNIT - II **10 hrs**

CAN DATA LINK LAYER
CAN data link layer – Principles of bus arbitration – Frame formats – Error detection &error handling – Extended frame format – Time triggered multiplexing
UNIT – III **10hrs**
CAN PHYSICAL LAYER
Physical signaling – Transmission media – Network topology – Bus medium access – Physical layer standards
UNIT - IV **10 hrs**
CAN PROTOCOL CONTROLLERS
CAN protocol controllers – Functions of a CAN controller – Message filtering – Message handling - Standalone CAN controllers – Integrated CAN controllers – CAN transceivers
UNIT – V **10 hrs**
CAN HIGHER LAYER PROTOCOLS
CAN application layer – Protocol architecture – CAN message specification – Allocation of message identifiers – Network management – Layer management – Higher layer protocols - CAN open – Device Net – SAEJ1939 – Time triggered CAN
TEXTBOOKS:
1. Konrad Etschberger, Controller Area Network , IXXAT Automation GmbH,2001
2. WolfhardLawrenz, CAN System Engineering: From Theory to Practical Applications, Springer,1997.

REFERENCE BOOKS:

3. GlafP.Feiffer, Andrew Ayre and Christian Keyold "Embedded Networking with CAN and CAN open".Embedded System Academy 2005.
4. Francoise Simonot-Lion, Handbook of Automotive Embedded Systems ,CRC Press,2007.
5. http://www.can-cia.org/can/
6. http://www.semiconductors.bosch.de/en/20/can/3-literature.asp

VLSI FOR WIRELESS COMMUNICATIONS	
23VE124(A)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisite:
Electronic Circuits, Electronic communication

COURSE OUTCOMES:
At the end of the course, students will be able to

1.	Learn about the Receiver Architectures like Receiver Front End, Filter Design
2.	Design and Analyze Low Noise Amplifier
3.	Design Active Mixer and analyze them.
4.	Analyze Passive Mixer and design for required parameters.
5.	Design Analog-to-Digital Converters for the required precision.

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	2	-
	2	3	2	3	2	-
	3	3	2	3	2	-
	4	3	2	3	2	-
	5	3	2	3	2	-

SYLLABUS

UNIT 1 **10hrs**

Receiver Architectures

Introduction, Receiver Front End, Filter Design, Rest of Receiver Front End: Nonidealities and Design Parameters, Derivation of NF, IIP 3 of Receiver Front End, partitioning of required NF rec _ front and IIP 3 rec _ front into individual NF, IIP 3

UNIT 2 **8 hrs**

Low Noise Amplifier

Introduction, Wideband LNA Design, NarrowBand LNA: Impedance Matching, Narrowband LNA: Core Amplifier.

UNIT 3 **10hrs**

Active Mixer

Introduction, Balancing, Qualitative Description of the Gilbert Mixer, Conversion Gain Distortion, Low Frequency Case: Analysis of Gilbert Mixer, Distortion, High-Frequency Case , Noise, A complete Active Mixer

UNIT 4 **12 hrs**

Passive Mixer

Introduction, Switching Mixer, Distortion in Unbalanced Switching Mixer, Conversion Gain in Unbalanced Switching Mixer, Noise in Unbalanced Switching Mixer, a practical Unbalanced Switching Mixer, Sampling Mixer, Conversion Gain in Single-Ended Sampling Mixer, Distortion in Single-Ended Sampling,

Intrinsic Noise in Single-Ended Sampling, Extrinsic Noise in Single Ended Sampling Mixer

UNIT 5 **10hrs**

Analog-to-Digital Converters

Introduction, Demodulators, A/D converters Used in a Receiver, Low-Pass Sigma-Delta Modulators, Implementation of Low-Pass Sigma-Delta, Bandpass Sigma-Delta Modulators, Implementation of Bandpass Sigma-Delta Modulators, I/Q mismatch in Mixer and A/D Converters.

Text Books:

"VLSI for Wireless Communications", 2nd edition, B. Leung, Springer-Verlag, 2011.

Reference Books:

1) Microelectronics circuits, Sedra and Smith 7th edition
2) Analysis and Design of analog integrated circuit, Gray, Meyer, Hurst, Lewis 5th ed

DESIGN FOR TESTABILITY	
23VE124(B)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites
Microcontrollers and Embedded Systems
OBJECTIVES:

3. To have knowledge in basic of data communication
4. To have a knowledge in Layers of CAN Network

COURSE OUTCOMES:

At the end of the course, students will be able to

1.	Learn about the basics Digital DFT and Scan Design.
2.	Illustrate the Built In Self-Test
3.	Illustrate the Boundary Scan standard
4.	Familiarize with AnalogTest Bus Standard
5.	Learn about the System Test and Core-Based Design

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	2	-
	2	3	2	3	2	-
	3	3	2	3	2	-
	4	3	2	3	2	-
	5	3	2	3	2	-

SYLLABUS

UNIT 1 **10 HRS**

TEST AND DFT FUNDAMENTALS

Introduction, The Definition of Testing, Test Measurement Criteria, Fault Modelling, Types of Testing, Manufacturing Test, Using Automatic Test Equipment, Test and pin timing, Manufacturing Test Program Components

UNIT 2 **10 HRS**

AUTOMATIC TEST PATTERN GENERATION FUNDAMENTALS

Introduction to Automatic Test Pattern Generation, The Reasons for ATPG, The Automatic Test Pattern Generation Process, Introducing the Combinational Stuck-At Fault, Introducing the delay Fault, Introducing the Current-Based Fault, Testability and Fault Analysis Methods, Fault Masking, Stuck Fault Equivalence, Stuck-At ATPG, Transition Delay Fault ATPG, Path Delay Fault ATPG, Current-Based Fault ATPG, Combinational versus Sequential ATPG, Vector Simulation, ATPG Vectors, ATPG-Based Design Rules, Selecting an ATPG Tool,

UNIT 3

SCAN ARCHITECTURES AND TECHNIQUES **10 HRS**

Introduction to Scan-Based Testing, Functional Testing, The Scan Effective Circuit, The Mux-D Style Scan Flip-Flops, Preferred Mux-D Scan Flip-Flops, The Scan Shift Register or Scan Chain, Scan Cell Operations, Scan Test Sequencing, Scan Test Timing, Safe Scan Shifting, Safe Scan Sampling: Contention-Free

Vectors, Scan-Based Design Rules, Stuck-At (DC) Scan Insertion,Stuck-At Scan Diagnostics, Scan-Based Logic BIST

UNIT 4

MEMORY TEST ARCHITECTURES AND TECHNIQUES 10 HRS

Introduction to Memory Testing, Memory Design Concerns, Memory Integration Concerns, The Basic Memory Testing Model, Scan Test Memory Modeling, Memory Test Requirements for MBIST, Memory Built-In Self-Test Requirements, An Example Memory BIST.MBIST Chip Integration Issues, MBIST Design—Using LFSRs.

UNIT 5

EMBEDDED CORE TEST FUNDAMENTALS 10 HRS

Introduction to Embedded Core Testing, What Is a Core?, What is Core-Based Design?, Core DFT Issues, Development of a ReUsable Core, DFT Interface Considerations—Test Signals, Core DFT Interface Concerns—Test Access, DFT Interface Concerns—Test Wrappers, The Registered Isolation Test Wrapper, The Slice Isolation Test Wrapper, The Isolation Test Wrapper—Slice Cell, The Isolation Test Wrapper—Core DFT Interface, DFT Interface Wrapper Concerns, DFT Interface Concerns—Test Frequency, Core DFT Development, Chip-Level DFT Integration Requirements

TEXTBOOKS:

1. Alfred L. Crouch, " Design-for-Test for Digital IC's and Embedded Core Systems."Prentice Hall PTR, 1999
2. Hideo Fujiwara , "Logic Testing and Design for Testability", MIT Press Series in Computer systems The MIT Press Cambridge, Massachusetts London, England, 1990

REFERENCE BOOKS:

3. Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen - VLSI Test Principles and Architectures_ Design for Testability (Systems on Silicon) (2006)

TESTING AND VERIFICATION OF VLSI CIRCUITS	
23VE124(C)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites
VLSI

COURSE OBJECTIVES

1. To provide an in-depth understanding of the testing and verification of faults affecting VLSI circuits.
2. To provide a basic idea on fault tolerance after testing.

COURSE OUTCOMES:

At the end of the course, students will be able to

1.	Learn about the VLSI testing principles, test equipment and testing economy
2.	Design the systems with DFT embedded within them.
3.	Illustrate the test generations methods and ATPG.
4.	Work on the BIST architectures to incorporate DFT
5.	Performs Boundary scan and core based testing

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	2	-
	2	3	2	3	2	-
	3	3	2	3	2	-
	4	3	2	3	2	-
	5	3	2	3	2	-

SYLLABUS

UNIT 1: **10 hrs**

Introduction to VLSI testing: Importance of testing, Challenges in VLSI testing, Levels of abstractions in VLSI testing, Functional vs. Structural approach to testing, Complexity of the testing problem, Controllability and Observability, Generating test for a single stuck at fault in combinational logic, D-algorithm, FAN and PODEM algorithms, Test optimization and fault coverage.

UNIT 2: **10 hrs**

Design for testability (DFT): Testability analysis, Scan cell design, Scan architectures, Scan design rules, Scan design flow, Special purpose scan designs Logic and fault simulation, Fault detection, Adhoc and structured approaches to DFT, Various kinds of scan design, Fault models for PLAs, Bridging and delay faults and their tests.

UNIT 3: **10 hrs**

Test generation: Random test generation, Boolean difference, ATPG algorithms for combinational circuits, Sequential ATPG, Untestable faults, IDDQ testing The LFSRs and their use in random test generation and response compression (including MISRs).

UNIT 4: **10 hrs**

Built-in self-test (BIST): Design rules, Exhaustive testing, Pseudo-random testing, Pseudo-exhaustive testing, Output response analysis, Logic BIST architectures Test compression: Test stimulus compression, Test response compaction, Architectures for test compression**.**

UNIT 5: **10 hrs**

Boundary scan and core based testing: IEEE standards for digital boundary scan, Embedded core test standards Analog and mixed signal testing, Delay testing, Physical failures, Soft errors Reliability, FPGA testing, MEMS testing, RF testing, High speed I/O testing.

TEXT BOOKS

1. Parag K. Lala, An Introduction to Logic Circuit Testing, Morgan & Claypool Publishers
2. Thomas Kropf, Introduction to Formal Hardware Verification, Springer

REFERENCE BOOKS

1. Michael L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing, Springer India
2. M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, Jaico Publishing House

HARDWARE SECURITY	
23VE124(D)	**Credits:3**
Instruction: 3 Periods	Sessional Marks:40
End Exam: 3 Hours	End Exam Marks:60

Prerequisites:, DICD using HDLs, DE, VLSI

Course Outcomes:

At the end of the course, students will be able to

1.	Analyze how digital system is specified, implemented, and optimized
2.	Explain VLSI testing
3.	Illustrate the hardware security and trust
4.	Detect and prevent hardware Trojans
5.	Counterfeit the ICs.

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	2	-
	2	3	2	3	2	-
	3	3	2	3	2	-
	4	3	2	3	2	-
	5	3	2	3	2	-

SYLLABUS

UNIT I **[10Periods]**

Digital System Design: Basics and Vulnerabilities:

Introduction, Digital System Specification, Digital System Implementation, Function Simplification and Don't Care Conditions, Sequential System Specification, Sequential System Implementation, Vulnerabilities in Digital Logic Design

UNIT II **[10 Periods]**

Back ground on VLSI testing:

Introduction , test cost and product quality , test generation, structural DFT techniques: Design for testability, Scan design, Partial scan design, Boundary scan, BIST methods, ,At-speed delay Test.

UNIT-III[9 Periods]

Hardware security and Trust:

Hardware Trojans: Implementation, Taxonomy, Detection methodologies, activation methodologies. Counterfeit ICs. Hardware Trojan Attack, Taxonomy.

UNIT IV **[10 Periods]**

Hard ware Trojan Detection and Prevention:

A Case Study for Hardware Trojan Detection in Third-Party Digital IP Cores ,Detection and Prevention at Register Transfer level, gate level

UNIT V **[10 Periods]**

Counterfeit ICs:

Taxonomy, Assessment, challenges, Path delay finger printing: degradation analysis, degradation analysis, finger print considering aging. Statistical data analysis, Process and temperature variation analysis.

TEXT BOOKS:

1. Mohammad Tehranipoor-Cliff wang editors, Introduction to hardware security and trust Springer Science & Business Media ,sep 2011
2. Mohammed Tehranipoor, Hassan salmani, Xuehui Zhang, Integrated Circuit Authentication ,Hardware Trojans and Counterfeit Detection,Springer International Publishing Switzerland 2014

ADVANCED MATHEMATICS	
23VE118(a)	**Credits:0**
Instruction: 3 periods	Sessional Marks:40
End Exam:	End Exam Marks:0

SYLLABUS

UNIT I **[10Periods]**

Linear Algebra-I:

Introduction to vector spaces and sub-spaces, definitions, illustrative example.Linearly independent and dependent vectors- Basis-definition and problems.Linear transformationsdefinitions. Matrix form of linear transformationsIllustrative examples

UNIT II **[10Periods]**

Linear Algebra-II:

Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases.Gram-Schmidt orthogonalization process.

UNIT-III **[10 Periods]**

Calculus of Variations:

Concept of functional-Eulers equation.Functional dependent on first and higher order derivatives, Functional on several dependent variables.Isoperimetric problemsvariation problems with moving boundaries.

UNIT IV **[10Periods]**

Probability Theory:

Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations.Poisson, Gaussian and Erlang distributionsexamples.

UNIT V **[10Periods]**

Engineering Applications on Random processes:

Classification.Stationary, WSS and ergodic random process.Auto-correlation functionproperties, Gaussian random process.

TEXT BOOKS:

1. B. S. Grewal, Higher Engineering Mathematics, 44/e, Khanna Publishers, 2017.
2. Erwin Kreyszig, Advanced Engineering Mathematics, 10/e, John Wiley& Sons, 2011.

Reference Books: 1. R. K. Jain and S. R. K. Iyengar, Advanced Engineering Mathematics, 3/e, Alpha Science International Ltd., 2002.
2. George B. Thomas, Maurice D. Weir and Joel Hass, Thomas Calculus, 13/e, Pearson Publishers, 2013

VLSI DESIGN LAB	
23VE126	**Credits:2**
Instruction: 3 Lab periods	Sessional Marks:50
End Exam: 3 Hours	End Exam Marks:50

Prerequisites:

Digital Electronics, VHDL, Verilog.

COURSE OBJECTIVES

- Familiarize with different VLSI design tools.
- Develop the ICs for digital applications with open source VLSI design tools.
- Prepare the prototypes.
- Testing the digital systems.
- Analyze the digital circuits.

COURSE OUTCOMES

After undergoing the course, students will be able to	
1	Work with TSPICE tools.
2	Design and verify various MOSFET Amplifier using SPICE mentor graphics tools
3	Design and verify various MOSFET Current Mirrors using SPICE
4	Design and verify MOSFET Gates using SPICE and mentor graphics tools

Mapping of Course Outcomes with Program Outcomes:

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3	3	-
	2	3	2	3	3	-
	3	3	2	3	3	-
	4	3	2	3	3	-

List of Experiments

PART – A

Design and simulate the following experiments with T SPICE

1. Design of Basic amplifier
2. Design of Cascode amplifier
3. Design of basic current sink
4. Design current Sink by using negative feedback resistor
5. Design of simple current Mirror
6. Design of Widlar Current Mirror
7. Design Of CMOS Inverter For A Switching Point Of Vdd/2
8. Estimate The Gain And Noise Margin Of CMOS Inverter
9. Find The Propagation Delay Of CMOS Inverter
10. Design A NAND Gate Using Pass Transistors And Draw The Vtc

PART -B

Design and simulate the following experiments with Cadence/Synopsis/ Mentor Graphics/equivalent EDA Tools

1. .Design and Simulate basic Common Source, Common Gate and Common Drain Amplifiers. Analyze the input impedance, output impedance, gain and bandwidth.
2. Design and simulate simple 5 transistor differential amplifier. Analyze Gain, Bandwidth and CMRR by performing Schematic Simulations.

TEXT BOOKS

1. B. Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill , 2002
2. P.E. Allen and D.R.Holberg, *CMOS Analog Circuit Design*, Oxford University Press , 2004

REFERENCE BOOKS

3. R.Gregorian and G.C.Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley and Sons , 2004
4. R.J.Baker, H. W. Li, D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, PHI , 2002

MIXED SIGNAL EMBEDDED SYSTEM DESIGN LAB	
23VE125	**Credits:2**
Instruction: 3 Practical & 3 O/Week	Sessional Marks:50
End Exam: 3 Hours	End Exam Marks:50

Prerequisites:

Before starting this course, students should have a basic idea of embedded systems and Internet of Things applications.

COURSE OBJECTIVES:

Students will understand the concepts of Internet of Things and can able to build IoT applications.

Course Outcomes:

(CO1) Implement basic output operations using a mixed signal reconfigurable embedded platform
(CO2) Design and verify digital and analog input operations using a reconfigurable embedded platform
(CO3) Design a real time embedded application with user input based operation.
(CO4) Design sensor and transducer based systems using a mixed signal embedded platform.
(CO5) Design advanced test and measurement systems using a reconfigurable mixed signal platform.

Mapping of Course Outcomes with Program Outcomes &Program Specific Outcomes:

		PO			PSO	
		1	**2**	**3**	**1**	**2**
CO	**1**	3	2	3		3
	2	3	2	3		3
	3	3	2	3		3
	4	3	2	3		3
	5	3	2	3		3

SYLLABUS

List of Experiments

1. simple LCD interfacing project to print "Hello World" using the PSoC 5 Platform. (CO1)
2. LED brightness control Fixed Function PWM Component of PSoC 5 Platform. (CO1)
3. Implementation of Interrupt based operation in PSoC 5 platform. (CO2)
4. Implementation of a Data Acquisition system Using Delta-Sigma ADC and UART components of PSoC 5 platform. (CO2)
5. Differential Mode Delta sigma ADC operation using PSoC 5 Platform.(CO3)
6. Reconfigurable on-chip multi-Op-Amp circuit design using PSoC 5 platform. (CO3)
7. Four Wire RTD based temperature measurement using PSoC 5 Platform.(CO4)
8. Simple USB Audio streaming application using PSoC 5 Platform. (CO4)
9. Implementation of a versatile signal generator using the WAVE DAC component of PSoC 5 (CO5)
10. implementation of a versatile signal current source using the IDAC component of PSoC 5 (CO5)
11. Design of a Boost converter using PSoC5 platform.(CO5)
12. Design of a Pseudo Random Sequence generator using PSoC 5 Platform.(CO5)
13. Implementation of a Quadrature Decoder using PSoC 5 Platform.(CO5)

Note: Students have to perform minimum of eight experiments (from Exp.1 to 11) and IoT based project.

Text Books:

2. Vijay Madisetti, ArshdeepBahga," Internet of Things A Hands-On- Approach",2014, ISBN:978 0996025515.

REFERENCE BOOKS:

1. Adrian McEwen, "Designing the Internet of Things", Wiley Publishers, 2013, ISBN: 978-1-118-43062-0
2. Daniel Kellmereit, "The Silent Intelligence: The Internet of Things". 2013, ISBN 0989973700.